IN THE CLAIMS

Please amend claims 31 and 34-36. All claims have been provided as a courtesy to the Examiner.

31. (Amended) A memory device, comprising:

a memory array;

a register [configured] to store at least one bit indicating a suspend status of a write operation; and

a control circuit coupled to said memory array and said register, said control circuit [is configured] to update said register and to control the output of a status signal representing said protection status of said data modification operation, and wherein said control circuit includes:

a first state machine [configured] to update at least one of said bits indicating said suspend status of said write operation in response to a suspend signal, and

a second state machine coupled to said first state machine and [configured] to control the output of said status signal in response to a status request signal.

32. (Unchanged) The memory device of claim 31, wherein said write operation represents a byte write operation.

33. (Unchanged) The memory device of claim 31, wherein said suspend signal represents a byte write suspend command.

34. (Amended) The memory device of claim 31, wherein said control circuit is [configured] to receive a status request signal and said register is [configured] to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (Amended) The memory device of claim 35, further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is [configured] to receive said status request signal from a processor and to provide said status signal to said processor.

36. (Amended) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is [configured] to provide a second status signal if [when] said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (Unchanged) The memory device of claim 31, wherein said status request signal is a read status register command.